Iterative Demapping and Decoding for DVB-S2 Communications

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Abstract. In this paper an original detection strategy for Satellite Digital Broadcasting communications is definited: particularly, we consider the DVB-S2 system, which is proposed as a development of the DVB systems and exploits iterative decoding and higher order modulation; these features allow the derivation of advanced detectors which are based on an iterative demapping and decoding approach. The adoption of this strategy approaches permits a remarkable performance gain and an improvement of the system throughput.

1 Introduction

Recently, the use of satellites in telecommunications has had a growing importance. The satellites are essential for linking users at large distance or in cases where cable connection is unpractical or uneconomic. Moreover, their use is essential in case of mobile users spread over a large area, in particular for aeronautical and maritime communications. Satellite systems give the opportunity of serving efficiently not uniformly distributed and asymmetric traffic due to the flexibility obtained by multiple and redirectable beams and to the possibility of dynamic reconfiguration of the resources. Finally, they allow to extend the range of terrestrial fixed and mobile networks. Satellite systems are mainly used in broadcasting and telephony, where they are especially suitable and efficient. Presently, the interest is focused on voice transmission, high definition video and picture transmission, wide band access to data, etc.

The DVB-S2 (*Digital Video Broadcasting* - *Satellite* - *Second Generation*) standard [4], proposed by DVB project[1], is a system aimed at providing a variety of satellite applications, higher power and bandwidth efficiency. The DVB-S2 system was introduced to improve the performance which is obtained by DVB systems; it is very flexible and its main characteristics are the following: a flexible input stream adapter, suitable for operation with single and multiple formats of the input streams, a powerful FEC system based on LDPC (Low-Density Parity Check) codes concatenated

[1] The Digital Video Broadcasting Project (DVB) is an industry-led consortium of over 270 broadcasters, manufacturers, network operators, software developers, regulatory bodies and others in over 35 countries committed to designing global standards for the universal delivery of digital television and data services.

with BCH codes, a wide range of code rates and 4 constellations optimized for non-linear trasponders. In the case of interactive and point-to-point applications, the ACM (Adaptive Coding Modulation) is adopted to optimize channel coding and modulation on a frame-by-frame basis. This technique provides more versatile and robust communications and a dynamic link adaptation to propagation conditions, targeting each individual receiving terminal.

The introduction of higher order modulation schemes permits to analyze the feasibility of a receiver which is based on the Iterative Detection and Decoding. In this paper, in order to ease the application of the Turbo principle, a well-known Turbo Code system, which has been previously considered in the DVB-RCS standard [5], has been introduced and tested. The proposed system permits to achieve remarkable results with a moderate complexity increase.

This paper is organized as follows. In Section II the system model is presented and the Turbo principle is described. Moreover the "tail-biting" technique and the "duo-binary" Turbo Codes are introduced and analysed. In Section III the behavior of the proposed receivers is discussed while in Section IV the simulation results are presented. The concluding remarks are given in Section V.

2 System Model

The successful proposal of Turbo codes [1] suggests the idea of an iterative (Turbo) processing techniques in the design of Satellite Digital Broadcasting communications. The considered Turbo Codes are composed of two Recursive Systematic Convolutional (RSC) codes connected by an interleaver.

Moreover, considering the flexibility of format of input stream and the wide range of code rates of DVB-S2 system, another structure is considered (see Figs. 1 and 2): while the former is used when the code rate is lower than 1/2, the latter is introduced for rates which are higher than 1/2. The two structures are different for the number of sistematic streams which are transmitted: while in the former case the data stream is only one, when the coding rates is higher than 1/2 the sistematic streams are two,

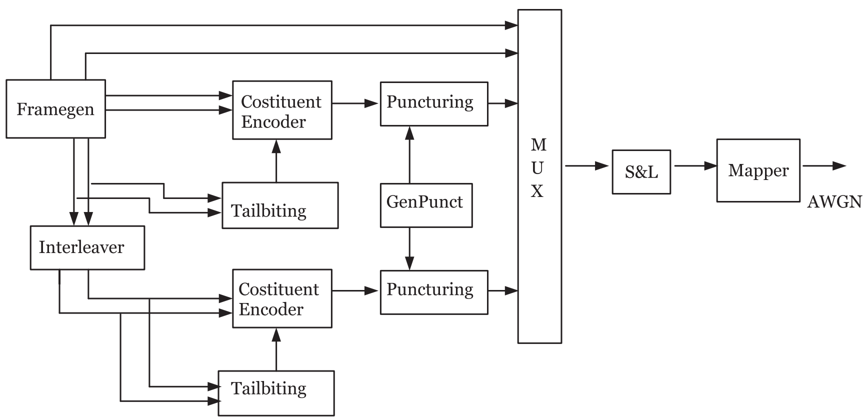

Fig. 1. Transmitter for DVB-S2 like system with rate >1/2.

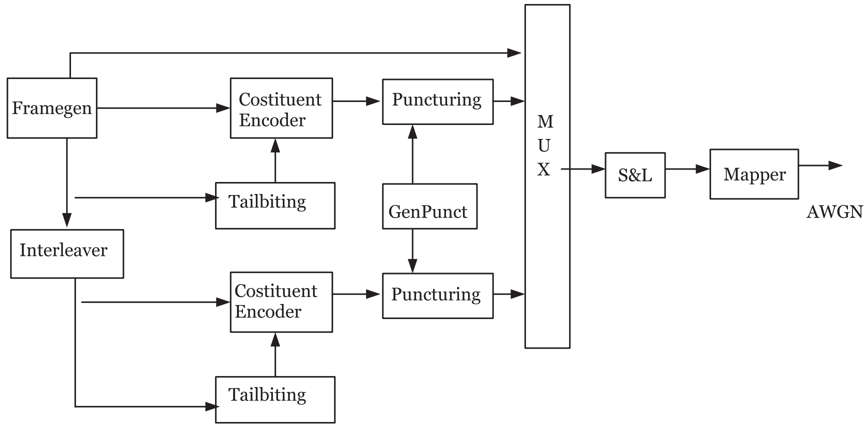

Fig. 2. Transmitter for DVB-S2 like system with rate < 1/2.

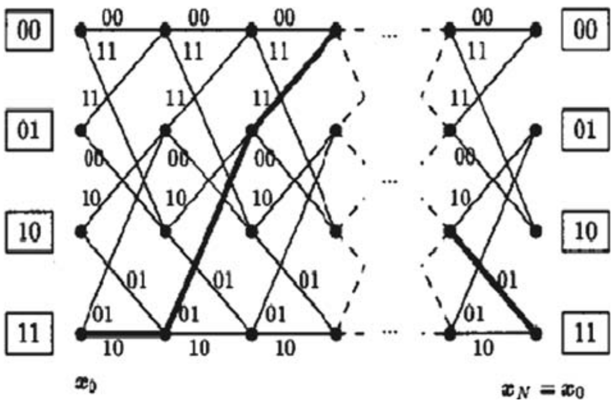

Fig. 3. Tail-biting technique.

that is the data input is a couple of bits. Two different Parallel Concatenated Convolutional Code (PCCC) encoders are so devised, one is a classical convolutional binary code while the other is a "'double-binary'" convolutional code [3]. Since the natural coding rate of the turbo encoder is equal to 1/2, a regular puncturing is performed at the output of the costituent encoders in order to obtain higher code-rate values. The costituent encoders call for the *tail-biting termination* technique so that the code trellis can be viewed as a circle (Fig. 3).

This transforms a convolutional code into a block code allowing any state of the encoder as the initial state and enconding the sequence so that the final state of the encoder is equal to the initial state [6]. There is no need to force the encoder back to the all zero-state by appending a block of tail bits to the information vector (zero termination): therefore the rate loss which is present in classical convolutional codes is avoided [7]. In the following, we describe a rate-k_0/n_0, $k_0 < n_0$, convolutional encoder as a device which generates the n_0-tuple

$$\mathbf{v}_t = \left(v_t^{(1)}, v_t^{(2)}, \ldots, v_t^{(n_0)}\right) \tag{1}$$

of code bits at time t given the k_0-tuple

$$\mathbf{u}_t = \left(u_t^{(1)}, u_t^{(2)}, \ldots, u_t^{(k_0)}\right) \tag{2}$$

The state of the encoder at time t is denoted by $\mathbf{x}_t = (x_t^{(1)}, x_t^{(2)}, \ldots, x_t^{(m)})$ where m is the number of memory elements of the encoder.

The correct initial state, which permits to fulfill the tail-biting boundary condition $\mathbf{x}_0 = \mathbf{x}_N$ can be calculated using the state-space representation

$$\mathbf{x}_{t+1} = \mathbf{A}\mathbf{x}_t + \mathbf{B}\mathbf{u}_t^T \tag{3}$$

$$\mathbf{v}_t^T = \mathbf{C}\mathbf{x}_t + \mathbf{D}\mathbf{u}_t^T \tag{4}$$

of the encoder, where $\mathbf{A}$ is the $(m \times m)$ state matrix, $\mathbf{B}$ denotes the $(m \times k_0)$ control matrix, $\mathbf{C}$ is the $(n_0 \times m)$ observation matrix, and $\mathbf{D}$ denotes the $(n_0 \times k_0)$ transition matrix.

The complete solution of (3) is given by the superposition of the zero-input solution $\mathbf{x}_t^{[zi]}$ and the zero-state solution $\mathbf{x}_t^{[zs]}$. The zero-input solution $\mathbf{x}_t^{[zi]}$ is the state achieved after t cycles if the encoding started in a given state $\mathbf{x}_0$ and all input bits are zero, whereas the zero-state solution $\mathbf{x}_t^{[zs]}$ is the resulting state at time t if the encoding started in the all-zero state $\mathbf{x}_0 = \mathbf{0}$ and the information word $\mathbf{u} = (\mathbf{u}_0, \mathbf{u}_1, \ldots, \mathbf{u}_{t-1})$ has been input. If we demand that the state at time $t = N$, that is after N cycles, is equal to the initial state $\mathbf{x}_0$, we obtain, after working (3), the equation

$$(\mathbf{A}^N + \mathbf{I}_m)\mathbf{x}_0 = \mathbf{x}_N^{[zs]} \tag{5}$$

where $\mathbf{I}_m$ denotes the $(m \times m)$ identity matrix.

Provided the matrix $(\mathbf{A}^N + \mathbf{I}_m)$ is invertible, the correct initial state $\mathbf{x}_0$ can be calculated from the zero-state response $\mathbf{x}_N^{[zs]}$. Therefore the encoding process can be divided into two steps:

- Firstly, the zero-state response $\mathbf{x}_N^{[zs]}$ for a given information word $\mathbf{u}$ is determinated. The encoder starts in the all-zero state $\mathbf{x}_0 = \mathbf{0}$; all $N\ k_0$ information bits are input while the output bits are ignored. After N cycles, the encoder is in the state $\mathbf{x}_N^{[zs]}$. We can calculate the corresponding initial state $\mathbf{X}_0$ using (5) and initialize the encoder consequently.
- The second step is the actual encoding. The encoder starts in the correct initial state $\mathbf{x}_0$ found in the first step; the information word $\mathbf{u}$ is input, and a valid codeword $\mathbf{v}$ is calculated.

In the following, we investigate the "Duo-binary Turbo codes" theory [8], [9], that is a generalization of the classical Binary Turbo Codes theory. In this case, generally, each component code rate was equal to 1/2 so that the resulting turbo code had a natural coding rate of 1/3. Obtaining higher rates involved puncturing the redundancy part of the encoded sequence. In cases where code rates higher than 1/2 are needed, especially when the turbo code is associated with high level modulation schemes, a better solution than puncturing involves component encoders able to encode 2 bits at the same time, that is "Duo-binary RSC encoders".

This structure can lead to improve the global performance in comparison with the original turbo codes, especially for block coding. In practice, for the construction of duo-binary turbo codes, we consider a parallel concatenation of two identical RSC encoders with 2-bits word interleaving (see Fig. 4). In order to encode data blocks without any rate loss or performance degradation due to direct truncating, the principle of circular trellises (tail-biting termination) is adopted. Figure 5 shows the structure of the costituent encoder that receives in input a couple of bits that is it said to be working at "symbol-level". As for the interleaver, the permutation function is performed on two levels:

– a *inter-symbol permutation* that modifies the order of symbols. This rule is almost regular. It is based on faint vectorial fluctuations around the locations given by regular permutation.
– a *intra-symbol permutation* that reverses bits in some prearranged couples.

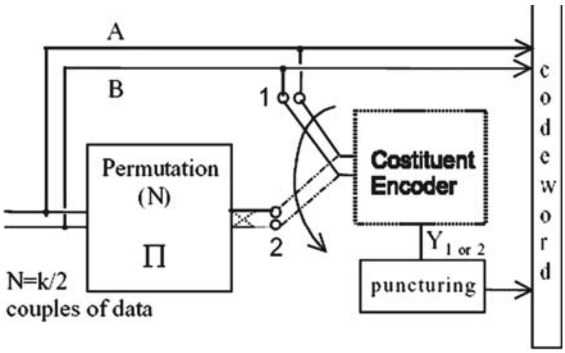

Fig. 4. Duo-binary turbo encoder.

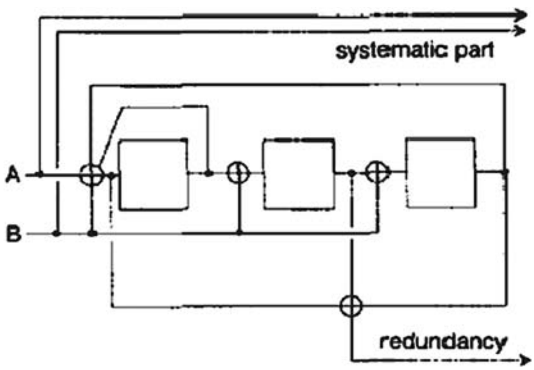

Fig. 5. 8-state quaternary recursive systematic convolutional (RSC) code with generators 15,13.

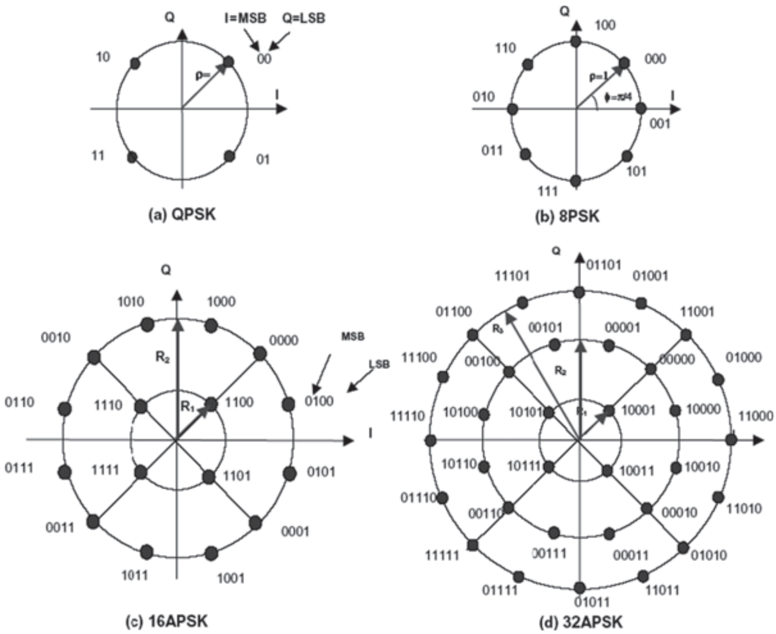

Fig. 6. Costellations of the DVB-S2 standard.

The encoded sequence, both in the structure for code rates higher than 1/2 and in that for code rates lower than 1/2, is multiplexed and it is sent to the mapper. The DVB-S2 standard provides for 4 costellations: the classical QPSK and 8PSK, and the 16APSK (amplitude and phase shift keying) and the 32APSK which allow to minimize the effects of the non-linear distorsion due to non-linear trasponders. To minimize these effects, new advanced pre-distortion methods are adopted in the up-link station. These modulations are based on concentric “rings” of equi-spaced points: 16 APSK is composed by a inner 4PSK surrounded by an outer 12PSK while 32APSK is composed by a inner 4PSK, by a 12PSK ring in the middle and by an outer 16PSK (see Fig. 6).

3 The Proposed Receivers

As for the transmitter, also for the receiver we propose two structures, one for code rates higher than 1/2 and the other for code rates lower than 1/2. Both structures rely on the iterative turbo decoding, which is based on the MAP algorithm. For every structure the canonical hard demapping, the soft demapping and the iterative soft demapping have been realized so as to show the improvements due to use of the different techniques (see Figs. 7, 8, 11, and 12).

In the case of Soft Demapping, the receiver requires soft information about reliability of both the systematic and the parity bits. The complex channel symbols are demapped by a log-likelihood ratio calculation for each of the M coded bits

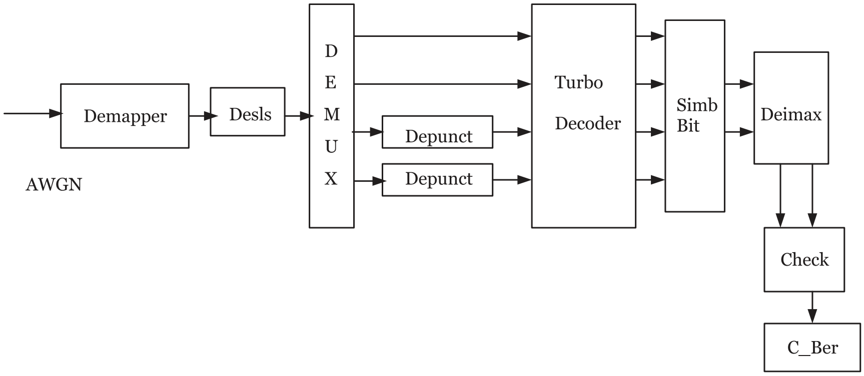

Fig. 7. Receiver with hard or soft demapping and iterative decoding for DVB-S2 like system with rate >1/2.

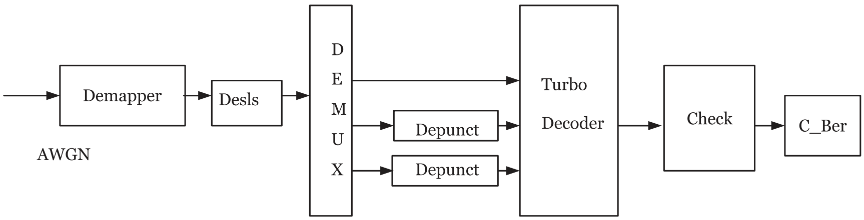

Fig. 8. Receiver with hard or soft demapping and iterative decoding for DVB-S2 like system with rate <1/2.

per symbol. Generally, the concept of Log Likelihood Ratios (LLRs) is useful to simplify the passing of information from one component decoder to the other in the iterative turbo decoding [10]. The LLR of a data bit c_i is denoted as $L(c_i)$ and is defined as the logarithm of the ratio of the probabilities of the bit taking its two possible values, ie:

$$L(c_i) \stackrel{\Delta}{=} \ln \frac{P(c_i = 1)}{P(c_i = 0)} \tag{6}$$

The sign of the LLR $L(c_i)$ of a bit c_i indicates whether the bit is more likely to be 1 or 0, and the magnitude of the LLR gives an indication of how likely it is that the sign of the LLR gives the correct value of c_i.

This concept proves useful also for the Soft Demapping. In this case the Demapper produces the conditional LLRs, $L(c_i \mid \mathbf{z})$, $i = 1, \ldots, M$, which can be calculated using the following expression [2]:

$$L(c_i \mid \mathbf{z}) = \ln\left(\frac{P(c_i = 1 \mid \mathbf{z})}{P(c_i = 0 \mid \mathbf{z})}\right) = L_{ap}(c_i) + \tag{7}$$

$$\ln\left(\frac{\frac{1}{\sigma^2}\sum_{j = bin1\,(i)} \exp\left(\left\|\mathbf{z} - y_j\right\|^2 + \sum_{k = other\,(j)} L_{ap}(c_k)\right)}{\frac{1}{\sigma^2}\sum_{j = bin0\,(i)} \exp\left(\left\|\mathbf{z} - y_j\right\|^2 + \sum_{t = other\,(j)} L_{ap}(c_t)\right)}\right)$$

where:

- $\sum_{j\,=\,bin1\,(i)}$ is referred to the symbols with the *i*th considered bit equal to 1.
- $\sum_{j\,=\,bin0\,(i)}$ is referred to the symbols with the *i*th considered bit equal to 0.
- $\mathbf{z}$ is the matched filter output.
- y_j is the *j*th considered symbol.
- $\sum_{k\,=\,other\,(j)}$ is referred to the other bits of the considered symbol that are equal to 1.
- $\sum_{t\,=\,other\,(j)}$ is referred to the other bits of the considered symbol that are equal to 0.

These values are called the *a posteriori* log-likelihood ratios.

After the Demapper, these soft values are passed to the iterative decoder composed by the two component decoders that are connected by the interleavers as shown in Figs. 9 and 10. At each new iteration, the iterative structure permits to allow an additional information to the first decoder in order to obtain a more accurate set of soft outputs, which are then used by the second decoder as *a priori* information. The structure for code rates lower than 1/2 works in the logarithmic domain while that for code rates higher than 1/2 works in the domain of the probabilities. In the latter case, since the structure uses the "Duo-binary Turbo codes" and so it works at "symbol level", the MAP algorithm is modified for producing the

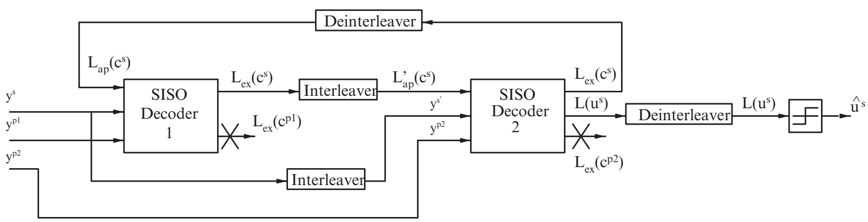

Fig. 9. Binary turbo decoder.

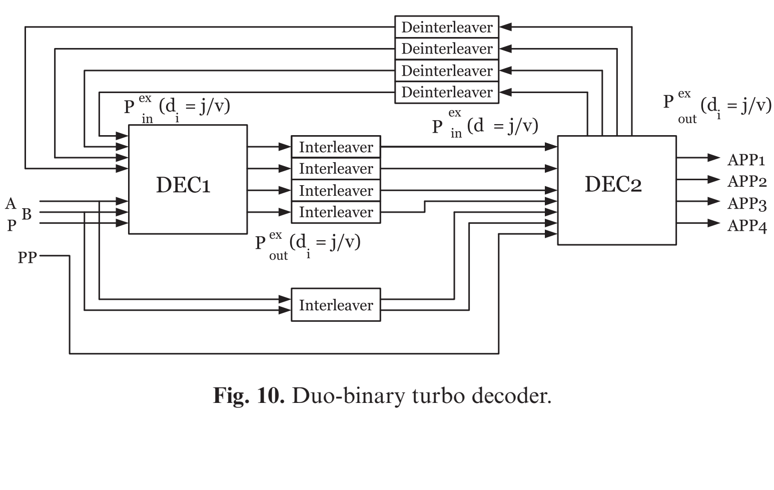

Fig. 10. Duo-binary turbo decoder.

a posteriori probability of each sistematic symbol. Moreover, also in the decoder, the permutation function of the interleavers and of the deinterleavers is performed on two levels.

In case of Iterative Soft Demapping, the decoding algorithm is properly modified to produce also the *extrinsic* information about the parity bits. The *extrinsic* information is obtained subtracting from the *a posteriori* information, the *a priori* information and the received systematic channel input. This relation is valid for sistematic and non-sistematic coded bits. After a fixed number of turbo decoder iterations, through the deinterleaver, the *extrinsic* information of coded bits at the output of the turbo decoder are fed back to the input of the soft demapping as the *a priori* information, $L(c_i)$, for the next receiver iteration, as shown in Figs. 11 and 12. The demapper can utilize the a priori information received from the decoder and calculate improved *a posteriori* values, $L(c_i \mid \mathbf{z})$, which are passed as *extrinsic* values to the decoder for further iterative decoding steps [2].

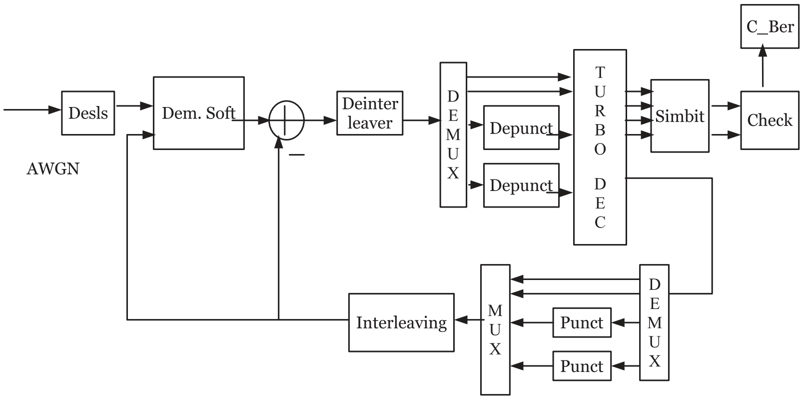

Fig. 11. Receiver with iterative soft demapping and iterative decoding for DVB-S2 like system with rate > 1/2.

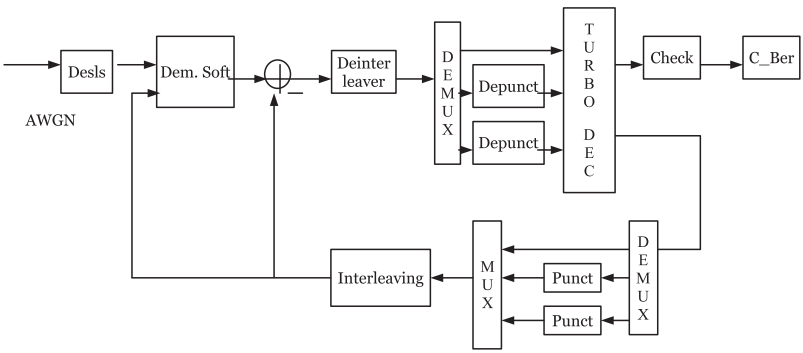

Fig. 12. Receiver with tterative soft demapping and iterative decoding for DVB-S2 like system with Rate < 1/2.

4 Simulations Results

In order to demonstrate the effectiveness and the performance of the proposed receivers, a set of computer simulations was performed.

For all simulations we used the *Log-MAP* Algorithm as decoding algorithm in the Turbo Decoder, since it permits to achieve very good performance but with a complexity lower than the MAP algorithm. The performance of the proposed receivers has been analyzed in a synchronous AWGN channel.

As shown before, we considered two structures: the former where code rates are lower than 1/2 and the latter where code rates are higher than 1/2. In the following we will separate these two cases also for simulation results.

In Fig. 13 we report the performance in terms of Bit Error Rate (BER) in case of QPSK modulation, rate equal to 1/3, soft demapping and iterative decoding. The performance has been analyzed for different values of the number of iterations of the turbo decoder. As the signal to noise ratio (SNR) grows, the value of BER decreases and the gain is more evident as the number of the iterations passes from 2 to 4, to 8 and to 10 iterations. The optimum value of the number of the decoding iterations results to be equal to 8. This occurs because, beyond this value, the additional information which can be obtain from the extrinsic information is lower.

In Fig. 14 we show the performance in terms of Bit Error Rate (BER) in case of QPSK modulation, rate equal to 1/3, iterative soft demapping and iterative decoding. In this case, we report the results as the total number of iterations changes.

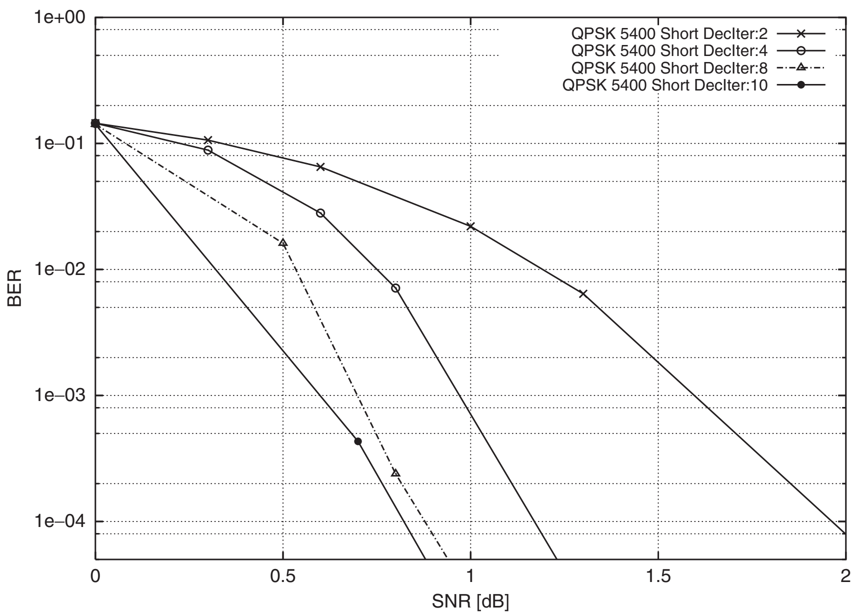

Fig. 13. Performance in terms of bit error rate (BER) for QPSK, rate 1/3, in case of soft demapping and iterative decoding.

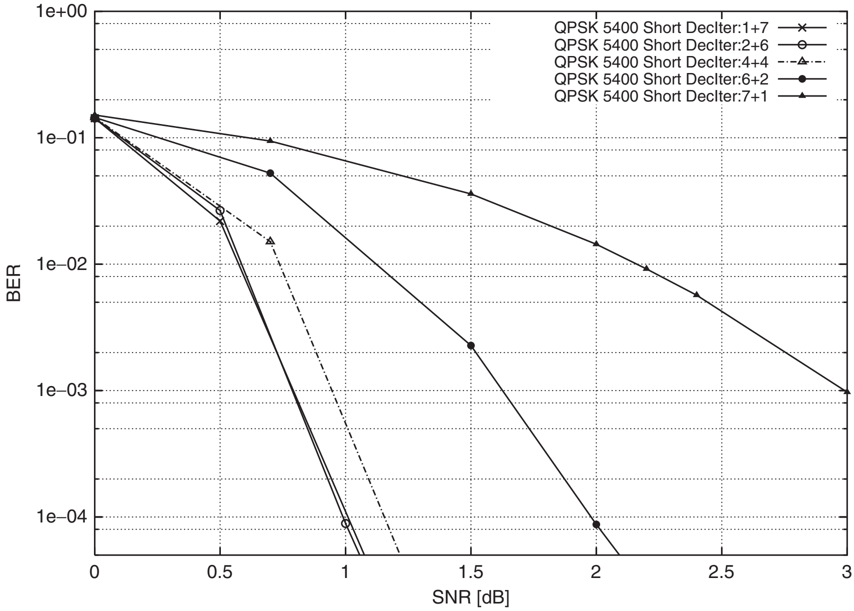

Fig. 14. Performance in terms of bit error rate (BER) for QPSK, rate 1/3, in case of iterative soft demapping and iterative decoding: 1 + 7, 2 + 6, 4 + 4, 6 + 2, 7 + 1 iterations.

As "total number" we mean the sum of the number of iterations of the turbo decoder before the outer demapping iteration and of the ones after the external iteration. We can observe which is the best strategy for realizing the iterative demapping. Indeed, the best results are obtained when few turbo iterations are performed before the external iteration of demapping and many turbo iterations are carried out after the iteration of demapping.

In Figs. 15 and 16 we report the performance comparison between hard demapping, soft demapping and iterative soft demapping in terms of Frame Error Rate (FER) and of net throughput for QPSK modulation with Gray mapping and code rate equal to 1/3. The considered total number of iterations is equal to 8. The soft demapping, both iterative and non-iterative, provides much better performance than the hard demapping. In this case no advantage is due to the iterative demapping in comparison with the non-iterative approach: this result depends on the mapping strategy which has been adopted and on the number of demapping iterations. The Gray mapping determines the independence of the bits in phase and in quadrature and so it is not possible to take advantage of the joint information of the bits belonging to the same symbol.

In the following we analyze some simulation results for the structure where the code rates are higher than 1/2. As shown before, this structure uses the duo-binary turbo codes: hence it was necessary to modify the decoding algorithm and the soft demapper.

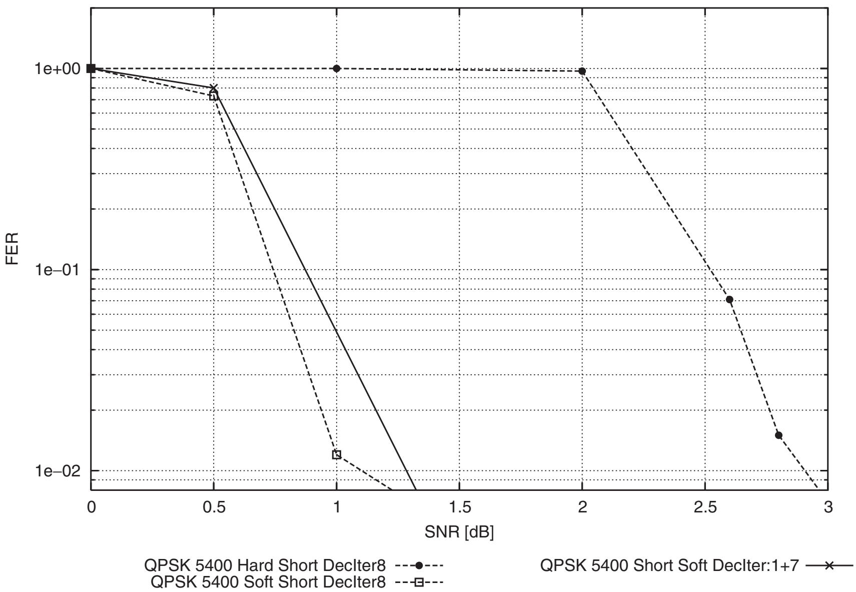

Fig. 15. Performance comparison in terms of frame error rate (FER) for QPSK, rate 1/3, between hard demapping, soft demapping and iterative soft demapping.

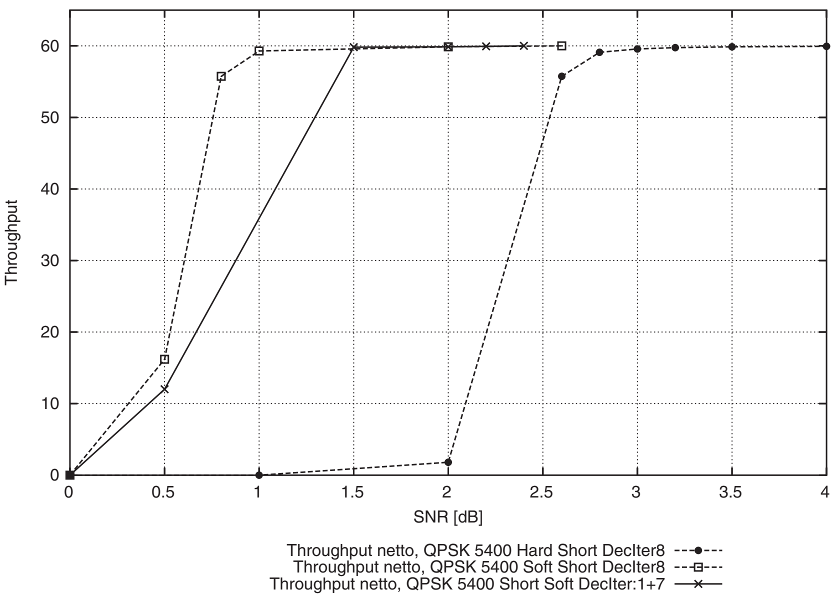

Fig. 16. Performance comparison in terms of net throughput for QPSK, rate 1/3, between hard demapping, soft demapping and iterative soft demapping.

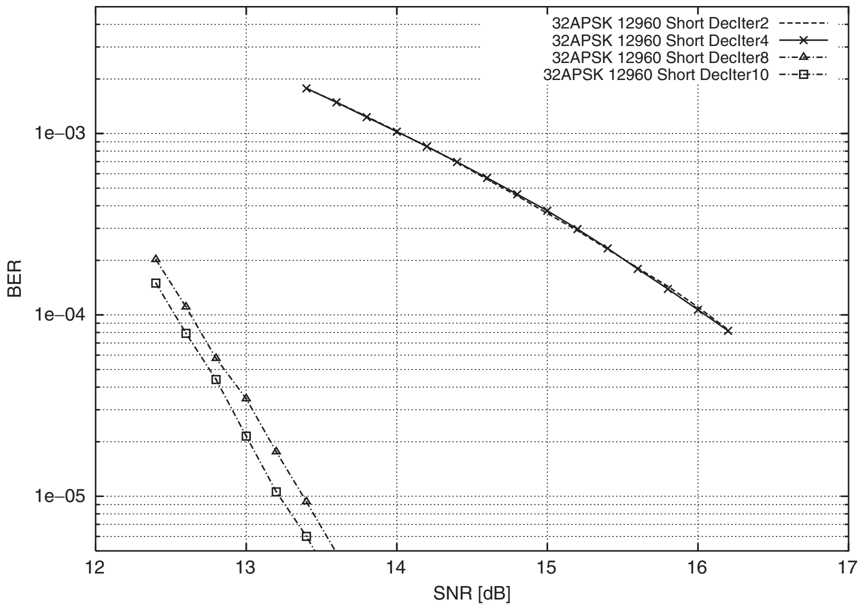

Fig. 17. Performance in terms of bit error rate (BER) for 32APSK, rate 4/5, in case of hard.

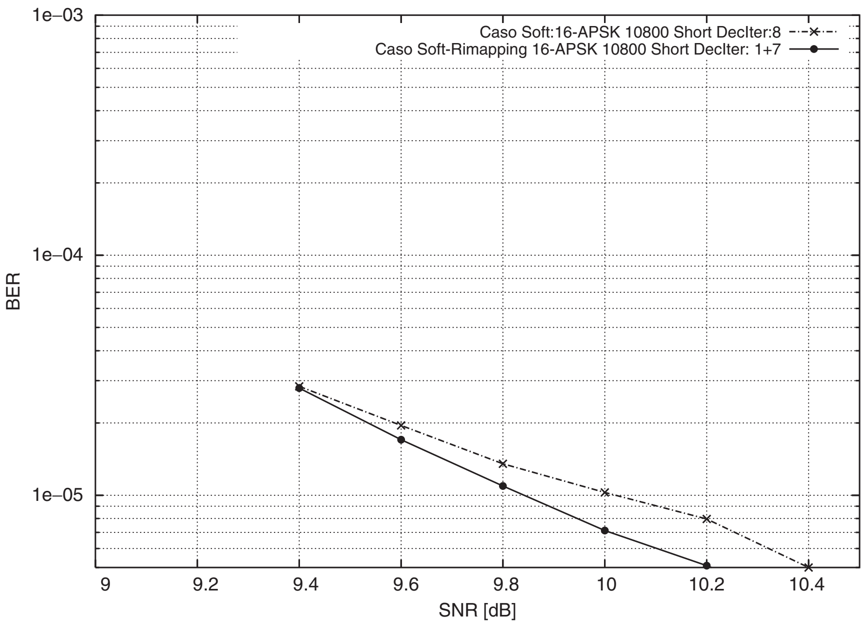

Fig. 18. Performance comparison in terms of bit error rate (BER) for 16APSK, rate 2/3, between soft demapping and iterative decoding.

In Fig. 17 we report the performance in terms of Bit Error Rate (BER) for 32APSK modulation, code rate equal to 4/5, hard demapping and iterative decoding. As in Fig. 13, as the signal to noise ratio grows, the BER decreases more quickly as the number of the iteration of the turbo decoder increases.

Finally, in Fig. 18, we show the comparison in terms of Bit Error Rate between non-iterative soft demapping and iterative soft demapping for 16APSK modulation and code rate equal to 2/3. In this case the iterative soft demapping behaves better than the non-iterative one, i.e., the iterative demapping produces some advantages. Since the 16APSK modulation does not present a Gray mapping it allows to exploit the joint information of bits belonging to the same symbol.

5 Concluding Remarks

In this paper we have proposed a novel detection strategy for satellite digital broadcasting systems. The advanced detectors which have been described, are based on an iterative decoding and on iterative and non-iterative demapping approach. The adoption of the soft demapping has presented a remarkable performance gain in comparison with the canonical hard strategy in all cases which have been analyzed. The advantages of the iterative soft demapping depend on the mapping strategy which is choosen and on the number of demapping iterations. The best performance is obtained when a non-Gray approach is considered.

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